COWLEY COLLEGE
& Area Vocational Technical School

COURSE PROCEDURE FOR

INTRODUCTION TO DIGITAL DESIGN
CIS_1894 4 Credit Hour(S)

Student Level:
This course is open to students on the college level in either the Freshman or Sophomore year.

Catalog Description:

CIS1894 – INTRODUCTION TO DIGITAL DESIGN (4 hrs)
This course will introduce students to various concepts in digital design. These topics include number systems, Boolean algebra, logic gates, gate-level minimization, combinational logic, synchronous sequential logic, registers and counters. The course consists of 3 classroom credit hours with 1 lab credit hour.

Prerequisites:
MTH4420 College Algebra or any math course above MTH4420.

Controlling Purpose:
This course is designed to provide an introduction to digital design. These concepts provide a foundation for future studies in courses related to engineering and computer engineering.

Learner Outcomes:
Upon completion of the course, the student will be able to demonstrate various methods of representing numbers in different systems, demonstrate various digital logic gates used in digital circuit design, find a minimal gate-level implementation of Boolean functions for a digital circuit, design and analyze circuits using combinational logic, design and analyze sequential circuits using combinational circuits and various memory elements, and design shift registers and counters.

Units Outcomes and Clock Hours of Instruction for Core Curriculum:
The following outline defines the minimum core content not including the final examination period. Instructors may add other material as time allows.

Evaluation Key:

A	=	All major and minor goals have been achieved and the achievement level is considerably above the minimum required for doing more advanced work in the same field.
B	=	All major goals have been achieved, but the student has failed to achieve some of the less important goals. However, the student has progressed to the point where the goals of work at the next level can be easily achieved.

C = All major goals have been achieved, but many of the minor goals have not been achieved. In this grade range, the minimum level of proficiency represents a person who has achieved the major goals to the minimum amount of preparation necessary for taking more advanced work in the same field, but without any major handicap of inadequacy in his background.

D = A few of the major goals have been achieved, but the student's achievement is so limited that he is not well prepared to work at a more advanced level in the same field.

F = Failing, will be computed in GPA and hours attempted.

N = No instruction or training in this area.

UNIT 1: Digital Systems and Binary Numbers

Outcomes: Demonstrate various methods of representing numbers in different systems

A	B	C	D	F	N	Specific Competencies
						Explain the binary number system
						Convert between binary, octal, decimal, and hexadecimal numbers
						Take the complement and reduced radix complement of a number
						Form the code of a number
						Form the parity bit of a word

UNIT 2 : Boolean Algebra and Logic Gates

Outcomes: Demonstrate various digital logic gates used in digital circuit design

A	B	C	D	F	N	Specific Competencies:
						Explain the basics of postulates used to form algebraic structures
						Explain the Huntington Postulates
						Use the basic theorems and postulates of Boolean algebra
						Develop a logic diagram from a Boolean function
						Derive a Boolean function from a logic diagram
						Apply DeMorgan's theorems
						Express a Boolean function as a truth table
						Derive a Boolean function from a truth table
						Express a Boolean function as a sum of minterms and as a product of maxterms
						Convert from a sum of minterms to a product of maxterms, and vice versa
						Form a two-level gate structure from a Boolean function in sum of products form; know how to form a two-level gate structure from a Boolean function in product of sums form
						Implement a Boolean function with NAND and inverter gates; know how to implement a Boolean function with NOR and inverter gates

UNIT 3: Gate-Level Minimization

Outcomes: Find a minimal gate-level implementation of Boolean functions for a digital circuit

A	B	C	D	F	N	Specific Competencies
						Derive and simplify a Karnaugh map for Boolean functions of 2, 3, and 4 variables
						Drive the prime implicants of a Boolean function
						Obtain the sum of products and the product of sums forms of a Boolean function directly from its Karnaugh map
						Create the Karnaugh map of a Boolean function from its truth table
						Use don't care conditions to simplify a Karnaugh map
						Form a two-level NAND and a two-level NOR implementation of a Boolean function
						Declare a Verilog module or a VHDL entity-architecture for a combinational logic circuit
						Write a structural model of the circuit for a given logic diagram using a) Verilog predefined primitives or b) user-defined VHDL components
						Draw the waveform of an input signal to the unit under test given a test bench

UNIT 4: Combinational Logic

Outcomes: Design and Analyze Circuits Using Combinational Logic

A	B	C	D	F	N	Specific Competencies
						Analyze a combinational logic circuit given its logic diagram
						Explain the functionality of a half adder and a full-adder
						Explain the concepts of overflow and underflow
						Describe the implementation of a binary adder
						Describe the implementation of a binary coded decimal (BCD) adder
						Describe the implementation of a binary multiplier
						Explain fundamental combinational logic circuits: decoder, encoder, priority encoder, multiplexer, and three-state gate
						Implement a Boolean function with a multiplexer
						Explain the distinction between gate-level, dataflow, and behavioral modeling with HDLs
						Write a gate-level Verilog or VHDL model of a fundamental logic circuit
						Write a hierarchical hardware description language (HDL) model of a combinational logic circuit
						Write a dataflow model of a fundamental combinational logic circuit
						Write a Verilog continuous assignment statement, or a VHDL signal assignment statement

						Declare a Verilog procedural block, or a VHDL process
						Write a simple testbench

UNIT 5 : Synchronous Sequential Logic

Outcomes: Design and analyze sequential circuits using combinational circuits and various memory elements

A	B	C	D	F	N	Specific Competencies:
						Explain how to distinguish a sequential circuit from a combinational circuit
						Explain the functionality of a SR latch, transparent latch, D flip-flop, JK flip-flop, and T flip-flop
						Use the characteristic table and characteristic equation of a flip-flop
						Derive the state equation, state table, and state diagram of a clocked sequential circuit
						Explain the difference between Mealy and Moore finite state machines
						Write a HDL model of the machine given the state diagram of a finite state machine
						Explain the HDL models of latches and flip-flops
						Write synthesizable HDL models of clocked sequential circuits
						Explain how to design a state machine using manual methods
						Explain how to eliminate equivalent states in a state table
						Define a one-hot state assignment code
						Design a sequential circuit with a) D flip-flops, b) JK flip-flops, and c) T flip-flops

UNIT 6 : Registers and Counters

Outcomes: Design shift registers and counters

A	B	C	D	F	N	Specific Competencies:
						Explain the use, functionality, and modes of operation of registers, shift registers, and universal shift registers
						Explain how to properly create the effect of a gated clock
						Explain the structure and functionality of a serial adder circuit
						Explain the behavior of a) ripple counter, b) synchronous counter, c) ring counter, and d) Johnson counter
						Write structural and behavioral HDL models of registers, shift registers, universal shift registers, and counters.

Projects Required:
The lab portion of the class will consist of the following labs (at a minimum):
1. Introduction to basic logic gates
2. Usage of NAND and NOR as universal gate
3. Implementing logic circuits using Boolean algebra concepts
4. Reduction and verification of Boolean expressions
5. Reducing SOP expressions using Karnaugh-Maps
6. Design and analyze binary to gray code converter
7. Design and analyze adders/subtractor using multism
8. Implementation of logic function
9. Verify the basic operation of D, JK and T FLIP FLOP
10. Design and implementation of 4-bit synchronous binary up counter

Textbook:
Contact Bookstore for current textbook.

Materials/Equipment Required:
None

Attendance Policy:
Students should adhere to the attendance policy outlined by the instructor in the course syllabus.

Grading Policy:
The grading policy will be outlined by the instructor in the course syllabus.

Maximum class size:
Based on classroom occupancy

Course Time Frame:
The U.S. Department of Education, Higher Learning Commission and the Kansas Board of Regents define credit hour and have specific regulations that the college must follow when developing, teaching and assessing the educational aspects of the college. A credit hour is an amount of work represented in intended learning outcomes and verified by evidence of student achievement that is an institutionally-established equivalency that reasonably approximates not less than one hour of classroom or direct faculty instruction and a minimum of two hours of out-of-class student work for approximately fifteen weeks for one semester hour of credit or an equivalent amount of work over a different amount of time. The number of semester hours of credit allowed for each distance education or blended hybrid courses shall be assigned by the college based on the amount of time needed to achieve the same course outcomes in a purely face-to-face format.

Refer to the following policies:

402.00 Academic Code of Conduct
263.00 Student Appeal of Course Grades
403.00 Student Code of Conduct

Disability Services Program:
Cowley College, in recognition of state and federal laws, will accommodate a student with a documented disability. If a student has a disability which may impact work in this class and which requires accommodations, contact the Disability Services Coordinator.